GENERAL INSTRUMENT

RO-3-9502

Program ROM

FEATURES

- Mask programable storage providing 2048 x 10 bit words
- 16 bit on-chip address latch
- Control decoder
- Programable memory map circuitry to place 2K ROM page within 65K word memory space located on 2K page boundaries
- Master logic with programable 16 bit vectored start address
- Interrupt logic with programable 16 bit vectored interrupt address
- 16 bit static address outputs for external memory
- Control signals for external memory:
  ENABLE = (DTB + DWS) Address External = R/$\overline{E}$
  WRITE = DWS. Address External = R/$\overline{W}$
- Programable memory map selection for external memory area
- Bus drive capability, 1 TTL load and 100pF plus tri-state

VIDEO

CIRCUIT REQUIREMENTS

The RO-3-9502 operates as the program memory for systems using a CP1610 series microprocessor.

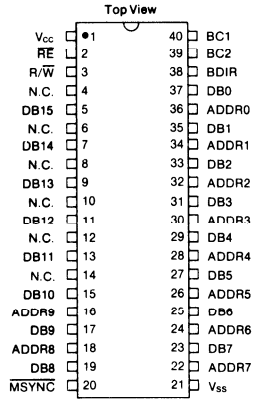
It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

OPERATING DESCRIPTION

The RO-3-9502 is initialized by the MSYNC Input and from the positive edge of this signal, it remains in a tri-state output condition, awaiting the IAB response. During the IAB, the 9502 transmits a 16 bit code onto the external bus thus providing the system start address vector. The completion of the MCLR sequence is recorded on chip such that any further IAB Codes output the second interrupt vector. From initialization, the 9502 waits for the first address code. For this address code and all subsequent address sequences, the 9502 reads the 16 bit external bus and latches the value into its address register. The contents of this address register are made available for connection to external memory and are supplied on 16 latched outputs with a drive capability of 1 TTL load and 100pF.

The 9502 contains a programable memory map location for its own 2K page and if a valid address is detected, the particular addressed location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the 9502 will output the 10 bits of addressed data and also drive a logic zero on the top six bits of the bus.

PIN CONFIGURATION
40 LEAD DUAL IN LINE



INPUT CONTROL SIGNALS

BDIR	BC1	BC2	EQUIVALENT SIGNAL	RESPONSE
0	0	0	NACT	NACT
0	0	1	IAB	IAB
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB
1	0	0	BAR	BAR
1	0	1	DWS	—
1	1	0	DW	—
1	1	1	INTAK	—

OPERATION WITH EXTERNAL MEMORY

The 16 bits from the address register are provided as static outputs for connection to external ROM or RAM devices. Two other signals are provided to control the external memory area. An enable signal is provided for any read or write operation, and a write signal, for any move out operation. The two external memory control signals are gated by a min-max memory map comparator. The minimum and maximum values are programable on boundaries within the 65K word memory area. The memory map comparator for external memory is a simple single compare and the operation is such that when a 2K area is chosen, a five bit compare is used and for a 4K area a four bit compare, etc. The effect of this is that 2K pages may start on 2K boundaries, i.e., 0, 2, 4, 6, 8 etc., but 4K pages must be on 4K boundaries, i.e., 0, 4, 8, 12, etc. The same is true for 8K and 16K pages.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

Standard Conditions (unless otherwise noted)

T_A = 0°C to +40°C V_{SS} = 0.0V
V_{CC} = +4.85V − +5.15V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs						
Input Logic Low	V_{IL}	0	—	0.7	volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	volts	
Input Leakage	V_{IL}	—	—	10	μA	$V_{IN} = V_{CC}$
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0.5	volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	+100pF
Address and Enable Outputs						
Output Logic Low	V_{OL}	0	—	0.5	volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	+100pF
Supply Current						
V_{CC} Supply	I_{CC}	—	—	120	mA	V_{CC} = 5.25V @ 40°C
AC CHARACTERISTICS						
Inputs						
Address Set Up	t_{as}	300	—	—	ns	
Address Overlap	t_{ao}	—	50	—	ns	
Write Set Up	t_{ws}	300	—	—	ns	
Write Overlap	t_{wo}	—	50	—	ns	
CPU BUS Outputs						
Turn ON Delay	t_{da}	—	—	300	ns	1 TTL Load
Turn OFF Delay	t_{do}	—	—	200	ns	+100pF
Address and Enable Outputs						
Turn ON Delay	t_{ad},t_{ed}	—	—	200	ns	
Turn OFF Delay	t_{eo}	—	—	150	ns	
Turn ON Delay	t_{wd}	—	—	300	ns	
Turn OFF Delay	t_{wo}	—	—	150	ns	

MEMORY TIMING RO-3-9502